REMARKS

Claims 1-48 are pending in the present application.

Claims 1-48 stand rejected under 35 U.S.C. §102(b) as being anticipated by Liencres et al. (U.S. Patent No. 5,434,993) (hereinafter "Liencres"). Applicant respectfully traverses this rejection.

Applicant's claim 1 recites

"A system, comprising:

a plurality of nodes coupled by an inter-node network, wherein each node includes a plurality of active devices, a memory subsystem, and an address network and a data network respectively configured to convey address packets and data packets **between** the plurality of active devices and the memory subsystem;

wherein a memory subsystem included in a node of the plurality of nodes is configured to maintain a response indication indicating whether the memory subsystem should send a data packet corresponding to a coherency unit in response to receiving from an active device in the node an address packet requesting an access right to the coherency unit;

wherein the node is configured to store **a node identifier** for the coherency unit, wherein **the node identifier identifies a different node** of the plurality nodes in which the coherency unit is in a modified global access state." (Emphasis added)

Applicant maintains the arguments made in the previous response to Office action dated May 3, 2007 to preserve them for appeal. Applicant makes the following additional arguments to further clarify why the claims distinguish over the cited art.

Applicant first notes that the Examiner, although allowed to interpret the art as broadly as is reasonable, has attempted to show that the system of Liencres, which

includes nodes coupled to a common memory, but which have an inherently different structure, is the same as the system claimed by Applicant. Applicant respectfully disagrees with both the structure and function.

More particularly, on page 2 of the present Office action, the Examiner responded to one of the Applicant's arguments regarding whether element 33 of Liencres could be construed to be Applicant's claimed address network. The Examiner asserts that it could because "The memory and processor are part of element 32 in Liencres, which is connected to element 33." Applicant respectfully disagrees with the Examiner's analogy. Specifically, as shown above, claim 1 explicitly recites "an address network and a data network, respectively configured to convey address packets and data packets between the plurality of active devices and the memory subsystem." Thus, the address network and data network are separate entities. This is absolutely not disclosed nor is it inherent in Liencres. As shown below, Liencres merely discusses that packets are sent, but does not indicate how. In addition, the Examiner asserts element 33 is coupled to element 32 which has the memory (according to the Examiner) and the processor. However, claim 1 requires that the address and data networks convey address and data packets between the active devices and memory. If, as the Examiner suggests, element 33 is the address network, then it is NOT conveying address packets between the active device and memory.

The Examiner further rebuts Applicant's arguments regarding whether the status bits of Liencres may be construed to indicate which node owns the coherency unit. The Examiner asserts that the status bits do identify the owner since they indicate/determine if the current node is the owner or not. Applicant submits that just because the status bits indicate the current node is or is not the owner, does not infer the status bits indicate which node is the owner.

Specifically, Liencres actually teaches at col. 7, lines 7-10

> "The bus cache controller 31 maintains a cache directory 46 containing the address tags and status bits for the data in the cache memory 37." (Emphasis added)

Liencres also discloses at col. 1 lines 61-65

> "To maintain cache consistency, several status bits are usually maintained in the cache directory which reflects the current state of the information in each cache line. Common status bits maintained include a "valid" bit, a "shared" bit, and an "owned" bit." (Emphasis added)

Liencres further discloses at col. 8, lines 12-24

> "when the processor 21 requires data that is not stored in the local cache memory 37, a cache miss occurs. The processor cache controller 35 issues a read request packet containing the required memory address to the bus cache controller 31 through the cache bus 33. As discussed in the read transaction section, the bus cache controller 31 responds to the read request packet by broadcasting a corresponding read request packet across the memory bus 25. The appropriate memory unit or processor subsystem on the memory bus 25 should eventually respond to the read request packet with a read reply packet containing the requested data." (Emphasis added)

Further, Liencres dislcoses in col. 7 "Read transactions"

> "When a memory request by the processor 21 cannot by fulfilled by the data in the processor cache memory 37, the processor cache controller 35 sends a read request packet across the cache bus 33 to the bus cache controller 31. The bus cache controller 31 proceeds to broadcast a corresponding read request packet across the memory bus 25. The read transaction initiated by the bus cache controller 31 consists of two packets: a read request packet sent by the bus cache controller 31 on the memory bus 25 and a read reply packet sent by another device on the memory bus. The read request packet contains the address of the memory requested by the processor cache controller 35 and is broadcast to all entities on the memory bus 25. A device on the memory bus 25 that contains the requested memory address responds to the read request packet with a read reply packet containing the subblock which includes the requested memory address. The read reply packet is generally issued by the main memory 23 except when the desired memory address is "owned" by another processor subsystem 20. In that case, the processor subsystem that owns the subblock must generate a read reply packet with the requested data."

Thus in addition to the arguments above, from the foregoing disclosure, it appears Liencres is merely stating that the cache controller maintains status bits for each cache line and the status bits are what one would customarily expect (e.g., valid, shared,

owned). However, the status bits do not indicate the node in which the coherency unit is in a modified global access state. There is absolutely no teaching of any node identifier that identifies a different node of the plurality nodes in which the coherency unit is in a modified global access state.

Liencres is also disclosing in response to a read request, eventually the owner will respond with the data. Further, in the Read transactions section, Liencres is only teaching that read requests are met with replies that contain the data, and that the bus controller 31 broadcasts the request (because there is no indication that identifes which node).

In the rejection of claim 1, the Examiner asserts element 31 is the address network and the data network. Applicant disagrees for the same reasons that element 33 cannot be the claimed address and data networks. The bus controller 31 is not an address and data network respectively, meaning separate. Liencres is silent as to the actual configuration of the bus controller. All Liencres teaches is that the memory bus 25 and the cache bus 37 are packet buses. There is no teaching whatsoever that there are separate address and data networks.

Further in the rejection of claim 1, the Examiner points to Liencres col. 7, lines 7-10 to teach the node identifier. Applicant disagrees and as already discussed above, that particular passage in Liencres merely discloses status bits in the cache directory, which do not indicate the node in which the coherency unit is in a modified global access state.

Thus, Applicant submits Liencres does not teach or disclose "each node includes and **an address network** and **a data network respectively** configured to convey address packets and data packets **between** the plurality of **active devices** and the **memory** subsystem;" and "wherein the node is configured to store **a node identifier** for the coherency unit, wherein the node identifier **identifies a different node** of the plurality nodes **in which the coherency unit is in a modified global access state**," as recited in claim 1.

Accordingly, Applicant submits claim 1, along with its dependent claims, patentably distinguishes over Liencres for the reasons given above.

Applicant's claim 17 recites features that are similar to the features recited in claim 1. Thus Applicant submits claim 17, along with its dependent claims, patentably distinguishes over Liencres for at least the reasons given above.

Claim 33 recites method comprising in pertinent part

"the node sending a coherency message requesting the access right to a different node of the plurality of nodes in response to **a node identifier identifying the different node** as a node in which the coherency unit is in a modified global access state."

As described above, these features are not taught in Liencres. Accordingly, Applicant submits claim 33, along with its dependent claims, patentably distinguishes over Liencres for the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-13501/SJC.

Respectfully submitted,

/ Stephen J. Curran /
Stephen J. Curran
Reg. No. 50,664
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

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